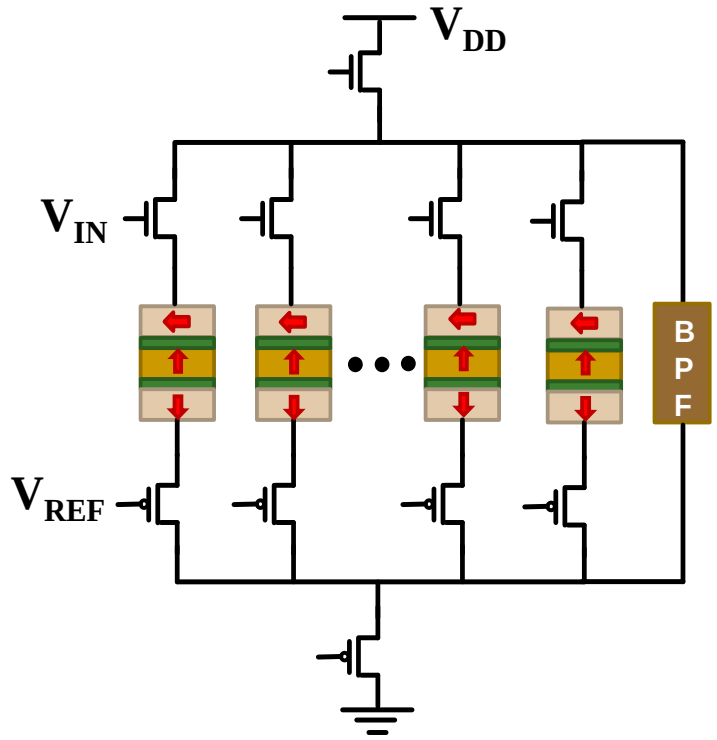


Our group focuses on research in the areas of high-performance and low-power very large scale integration (VLSI), temperature-aware circuits and architecture, embedded systems, and nanoelectronics. Below several sample projects are described which demonstrate the breadth of interests in our lab.

# hplp Lab

High-Performance Low-Power


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## High-Performance Low Power (HPLP)

The High-Performance Low-Power (HPLP) Laboratory is dedicated to research in the area of Very Large Scale Integrated (VLSI) Circuit design. Ongoing research ranges from power-, temperature-, and reliability-aware CMOS circuit design to explorations in spintronics and nanoelectronics.

## Nanoelectronic Circuits

We are seeking to reduce by orders of magnitude the power/energy of nanoelectronics by exploiting the very steep subthreshold swings achievable with metal insulator transition metals (Mott insulators) to develop, optimize, and fabricate devices and circuits that work with power supplies in the millivolt range.

## Temperature-Aware Circuits and Architectures

Process, Voltage, Temperature, and Aging variations are some of the most serious roadblocks facing the semiconductor industry in its quest for ever higher levels of integrations, better performance, and lower power consumption. Variations reduce yields and performance at higher power and cost.

## Cross-Layer Accelerated Self-Healing (CLASH)

Aging of ICs is a long term process caused by several interrelated physical mechanisms that make circuits slower and increase power leakage. Aging consists of both reversible and irreversible phenomena. When the system is not stressed there is some level of recovery, typically at much lower rate than the wearout. We are working to improve the lifetime as well as power, performance, and area metrics of future electronic systems by the use of extensive and accelerated recovery methods for aging mechanisms such as bias temperature instability for CMOS and program/erase wearout for flash. Ultimately, we seek to optimize conditions such that it is possible to deeply rejuvenate electronic systems periodically so they provide more value to the user.

## SpinTop – Computing with Spin-Torque Nano-Oscillator (STNO) Arrays

As conventional CMOS technologies are running into multiple "red brick walls" there is a need for new material discoveries and new nanodevice and circuit paradigms that allow new applications that would be impractical or even impossible using traditional methods. Coupled STNO arrays are a very low power computing fabric that can be integrated with CMOS, have tunable frequency, high quality factor, can have their coupling controlled using multiferroics to be used in many applications, from RF filters and mixers, to onchip clock generation, to biologically-inspired nonBoolean computation.

## Breaking the 3D power delivery walls using voltage stacking

The power delivery walls include: power density (power consumption density beyond the heat dissipation capabilities of the technology), power and ground delivery pins (chip power consumption requires increasing numbers of pins), 3DIC power density (the third dimension exacerbates the two-dimensional explosion), onchip regulation efficiency (poor efficiencies achievable onchip limit the effectiveness of many low power schemes). Voltage stacking is a comprehensive method for addressing the power delivery walls above.

## RECENT RESEARCH DEVELOPMENTS

- Designed novel hybrid MTJ/spinvalve structure that results in a highly harmonic STNO with high output signal
- Designed novel electrical coupling method for STNO arrays that allows arrays with arbitrary topologies
- Demonstrated accelerated aging and recovery on commercial SRAM and FPGA ICs

## RECENT GRANTS

- SRC/NSF – CLASH: Cross-Layer Accelerated Self-Healing: Circadian Rhythms for Resilient Electronic Systems
- NSF – EAGER: Nano-Patterned Coupled Spin Torque Oscillator (STO) Arrays – a Potentially Disruptive Multipurpose Nanotechnology
- ATK – Distributed GNU Radio

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