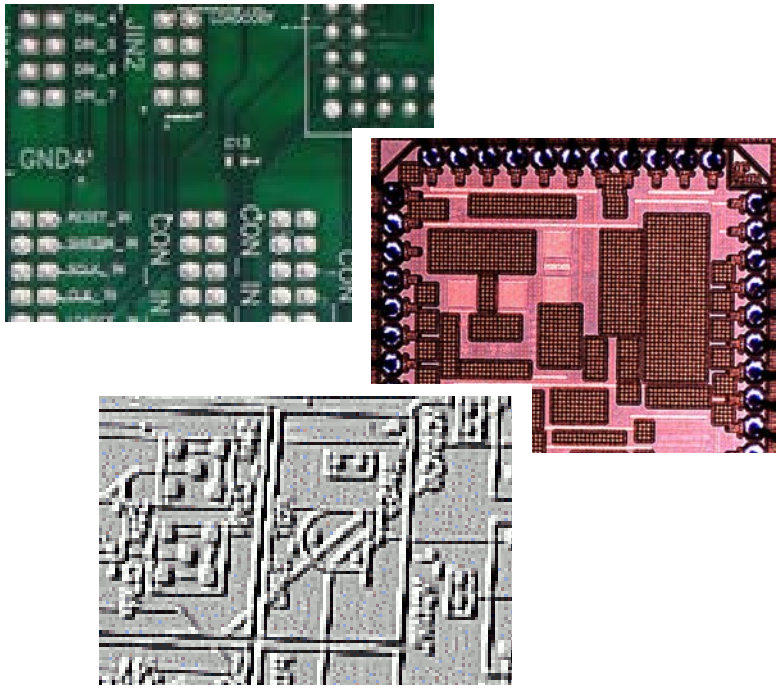

Our group investigates research topics related to modern VLSI design. Among the many challenges facing circuit designers in deep sub-micron technologies, power and variation are perhaps the most critical. Our group's focus is to confront these problems in a range of applications and different regions of the design space. Our specific research interests include low power digital circuit design, sub-threshold digital circuits, SRAM design for end-of-the-roadmap silicon, variation tolerant circuit design methodologies, and medical applications for low energy electronics.

Robust Low Power VLSI Group

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"Solving the research problems to allow the development of new technologies which harvest and use extremely low amounts of energy."

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SRAM

Static Random Access Memory (SRAM) is a critical component in most VLSI systems. Our group is working on several issues related to SRAM including:

- SRAM design Automation – We have developed a virtual prototype (ViPro) which enables iterative SRAM design space exploration to facilitate optimal, sub-45nm SRAM designs.
- Circuit assist methods for nanoscale SRAM – Large scale 6T SRAM beyond 65nm increasingly rely on assist methods to overcome the functional limitations associated with scaling and the inherent read stability/write margin tradeoff. We have developed a margin/delay analysis of bias based circuit assist methods, highlighting the assist impact on the functional metrics, margin and performance.
- Dynamic stability- We are investigating and characterizing cell read and write stability using dynamic margins which allow for a more realistic view of operations.
- High reliability SRAM for extreme environmental conditions – We are investigating circuit and architectural techniques to improve the reliability of SRAM at extreme temperatures, particularly for automotive applications.
- Alternative bitcells - In order to improve bitcell robustness (improve ready static noise margin and write noise margin), we are exploring several alternative bitcell structures.
- Nanoscale CMOS SRAM device technology – Reduced device dimensions and operating voltages that accompany technology scaling have led to increased design challenges with each successive technology node. We are using a combination of TCAD and circuit simulation tools to explore the role of technology scaling on shaping the future of SRAM bit cell design. Additionally, we are investigating the sources of non-random device mismatch in future nanoscale SRAM devices.

Body Sensor Networks

Body area sensor networks (BASN) are rapidly becoming important tools in today's health care. However, this trend is constrained by flexible on-node processing and very long device lifetimes. We seek to increase life times of these devices resulting in reduced cost to consumer and less invasive procedures to replace batteries/nodes. We are utilizing low power RF transmitters, low voltage boost circuits, subthreshold processing, biosignal front-ends, dynamic power management, and energy harvesting to realize an integrated reconfigurable BASN SoC capable of autonomous power management for battery-free operation.

Energy Efficient Circuits

We are researching Panoptic Dynamic Voltage Scaling (PDVS) as an approach to ultra-low power (ULP) design to reduce energy without sacrificing performance. We are looking at this and other advanced power distribution methods and their effect on the on-chip power network. We are also exploring the use of reconfigurable circuits for ULP devices, miniature devices. Lastly, we are exploring the uses and limitations of RFID tags.

RECENT RESEARCH DEVELOPMENTS

- Demonstrated a 19μW wearable body sensor for ECG / EEG / EMG with sensing, processing, memory, power harvesting, power management, and a radio for wireless communication.
- Leading the integration thrust in a new NSF Engineering Research Center called ASSIST, which is developing self-powered wearable sensors.

RECENT GRANTS

- NSF – NSF Nanosystems Engineering Research Center for Advanced Self-Powered Systems of Integrated Sensors & Technology (ASSIST)
- ONR – Detection/Tracking of Submerged Hyrdrodynamic Wakes Using a Bioinspired Hybrid Fluid Motion Sensor Array
- ONR – Development & Testing of an Ultra Low Power System-on-Chip (SOC) Platform

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